COMPARATIVE ANALYSIS OF SERIAL VS PARALLEL LINKS IN NOC

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ABSTRACT

Analytical model is employed to characterize and compare serial and parallel communication techniques in NoC interconnect. Simulations that are based on 130nm and 70nm technology parameters reveal up to ×5.5 and ×17 reduction in power and area of serial vs. 32-bit multi-layer parallel link, respectively. Lower power is dissipated by a single-layer parallel link but it occupies larger area. We conclude that long on-chip interconnects could benefit from serial links.

I. INTRODUCTION

Large Systems-on-Chip (SoC) can employ packet-switched Networks on-Chip (NoC) [1]~~[1]~~. Typically, NoC is based on module connection via a mesh-type network of routers. NoC allows design modularity and high level of abstraction in architectural modeling of the system.

Transportation of data packets in NoC is currently performed by using multiple parallel links, which are proven more efficient than buffers-based architectures [2]~~[2]~~. However, this technique incurs a high area cost, when inter-wire spacing, shielding and repeaters are considered. The area can be minimized when multiple metal layers are employed, but using repeaters increases the required area resources due to via blockage [6]~~[6]~~ and repeater sizes.

Serial links for NoC data transport have been proposed to overcome the drawbacks of parallel links [3]~~[3]~~[4]~~[4]~~[5]~~[5]~~. They should not only allow savings in wire area and power dissipation and reduction of signal interference, noise and crosstalk, but also eliminate the need for multiple line drivers and buffers. Thus, serial links may be area-efficient not only at the interconnect level, but also at the circuit level, despite the required addition of a serializer and deserializer.

Additional advantages of serialization include the elimination of skew uncertainty thanks to removal of multiple signal wires; layout and timing verification simplicity; blockage reduction thanks to reduced number of vias and repeaters; and throughput control through changing of serializer frequency. Potential limitations of serial links, such as increased ISI between successive signals and the need for high-speed operation, can be addressed by encoding and asynchronous communication protocols.

In this paper we present the comparative analysis of serial and parallel links. The techniques are compared based on technology parameters, showing power and area consumption versus length and throughput requirements of the link. We present detailed models of both circuitry and wire components. Analytical models and simulation results are followed by conclusions and future research directions.

II. SERIALIZER STRUCTURE

The transformation of parallel multi-bit signal flow into a serial line and vice-versa requires special units at both ends of the link. The Serializer and De-serializer interface the router/module to the serial link. The serializer converts *m*-bit parallel data into serial form. It must operate at high speed to compensate for the loss of parallelism. This creates a challenging trade-off between transistor scaling and compact, low-power implementation.

The serializer is based on a switch array, and can be controlled by either a Muller pipeline [7]~~[7]~~ initiated by system clock pulses for asynchronous protocols, or by synchronous multiplexer controlled by a fast clock. The advantage of the asynchronous implementation is in high-speed operation without a need for *m*-times faster clock generation with high area and power consumption. The serializer can be designed for various lane width scenarios, or as a generic unit with lane width controller applied to the multiplexer and switch array. In this paper we consider only two cases: a fully parallel link and a single-wire serial link.

III. ANALYTICAL MODELS

Both serial and parallel links are modeled according to Figure 1~~Figure 1~~ and parameters are derived using the analytical expressions presented in this Section.

Serial Link - The delay of the serializer is calculated as the sum of gate delays. For a capacitive load, the gate delay is expressed by the Logical Effort method [9]~~[9]~~:

$$D_{gate} = \tau \cdot (gh + p) \tag{1}$$

where τ is a technology-dependent time constant, g is the logical effort independent of transistor sizes, h is electrical effort and p represents the parasitic delay of the gate. Transistors sizes are increased when delay must be minimized to meet throughput demands.

Link optimization by repeater insertion is performed in three stages.

a) Repeaters and cascade driver are modeled using [10]~~[10]~~:

$$k_{rep} = \sqrt{\frac{0.4 \cdot C_{int} R_{int} \cdot L^2}{0.7 \cdot R_{t_{inv}} \left(C_{t_{inv}} + C_{pt} \right)}}, \quad h_{rep} = \sqrt{\frac{C_{int} R_{t_{inv}}}{C_{t_{inv}} R_{int}}} \tag{2}$$

$$k_{cas} = \log\left(\frac{h_{cas} \cdot C_{t_{inv}}}{C_{drv}} \right), \quad h_{cas} = \ell$$

where k are counts and h are scaling factors of devices. C_{drv} assumed to be the input capacitance of the first repeater and C_{int} and R_{int} are the wire capacitance and resistance per unit of length.

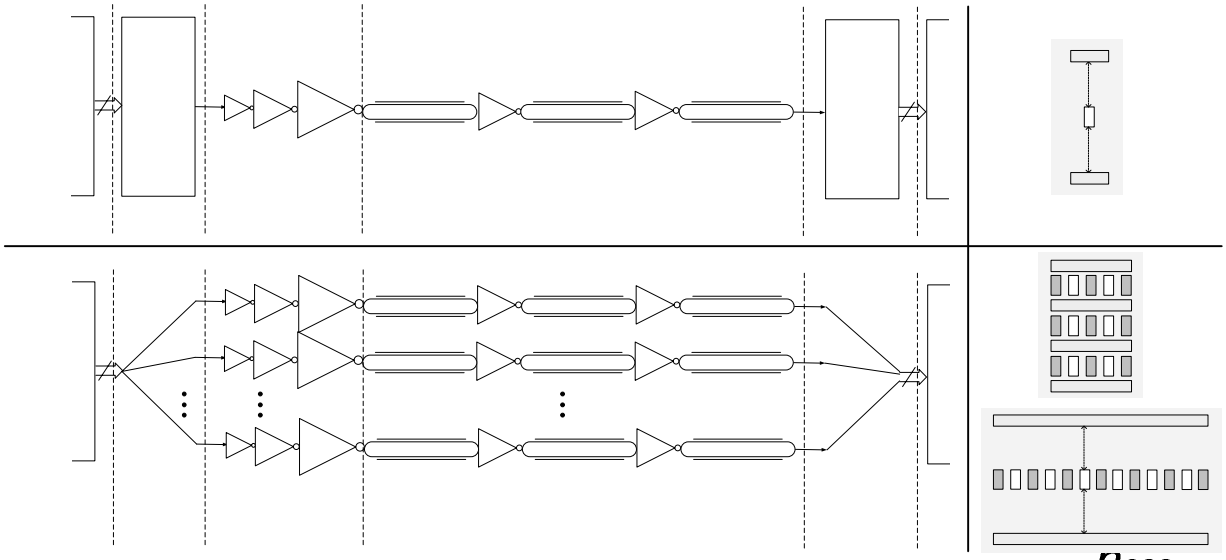

Figure 1. *Serial and Parallel link architectures, related parameters and wire structures.*

b) Power is minimized by scaling repeaters while having minimal impact on delay as described in [11][11][15][15][19][19]. Delay is calculated using Logical Effort method [9][9] for gates and repeaters and using Elmore delay model [20][20] for interconnect. The delays of the i^{th} repeater-interconnect segment are [12][12]:

$$D_{gate} = \tau \cdot \left(g_i \cdot \left(\frac{C_{i+1} + C_{w_i}}{C_i} \right) + p_i \right) \qquad (3)$$

$$D_{interconnect} = R_{w_i} \cdot \left(0.5 \cdot C_{w_i} + C_{i+1} \right)$$

C_i and C_{i+1} are input capacitance of gates i and $i+1$ respectively, while Cw_i and Rw_i are the wire capacitance and resistance of segment i.

c) Throughput-centric optimization is applied to wires and repeaters as in [13][13]. The throughput-per-unit-area is:

$$T_A = \frac{1}{D_{link}(W+S)L} \qquad (4)$$

where S is metal spacing and W is wire width. Maximal throughput per unit area is achieved iteratively by calculating optimal wire width using the partial derivative of (4) with respect to W and finding the resulting count and size of the repeaters. The outcome of this third and final stage is employed in the following simulations.

The serial wire is placed in an intermediate metal layer to maximize the distance to the neighboring wires and supply lanes. In this way the capacitance of the serial wire is minimized allowing high-speed operation.

Parallel Link - A 32-bit parallel link is employed with full shielding [14][14][15][15]. The two upper metal layers are used for power distribution and the remaining layers are fully shielded, leaving four or three effective layers for signal distribution (in 130nm or 70nm, respectively). Wire width and repeater parameters are scaled down from the optimum in order to meet the reduced throughput demands of each wire in the link (relative to the serial wire). This is applied iteratively considering the reduced throughput:

$$T_{parallel} = \frac{T_{serial}}{N_w} \qquad (5)$$

where N_w is the number of parallel wires in the link. Thanks to the reduced throughput, parallel links dissipate lower power than the serial ones.

Two types of parallel link structures are considered in the analysis – a typical high-performance multi-layer structure, where signal and shield wires alternate and adjacent layers are used as either perpendicular signal wires [15][15] or as ground planes [16][16], while forming waveguides with minimized crosstalk, noise and impedance; and a low-power structure where all signal wires are located in a single intermediate metal layer to reduce capacitance, similar to the serial wire.

Power - Total power dissipation of the link is defined by:

$$P_{link} = P_{SerDes} + P_{drivers} + P_{repeaters} + P_{wires} \qquad (6)$$

(parallel links do not include power dissipation of the serializer and de-serializer). Each power factor can be defined as the sum of dynamic and leakage power components using:

$$P_{dyn} = \alpha \cdot C \cdot V_{DD} \cdot f \qquad (7)$$

$$P_{leak} = W_{tot} \cdot V_{DD} \cdot I_{off} \qquad (8)$$

where α is the activity factor, W_{tot} is the total width of the devices and I_{off} is the off-current per device width [18][18]. The short-circuit power is relatively minor and can be neglected.

P_{dyn} in parallel wires is calculated for a reduced frequency f according to (5). P_{leak} is estimated using data of [17][17] where leakage current per device width grows dramatically from 0.01μA/μm in 130nm to 0.05μA/μm in 70nm, and is predicted to continue growing with the advent of technology.

Area – Link area is estimated assuming a factor of ×5 for average device size relative to its $W \times L$ gate size. The area of wires including repeaters is the maximum of repeaters area and the vertical projection of the wiring:

$$A_{link} = A_{SerDes} + A_{drivers} + \max\left(A_{repeaters}, A_{wires} \right) \qquad (9)$$

This method defines the effective blockage of area resources, while accounting for the multi-layer structure of the parallel link.

IV. ANALYSIS SETUP AND RESULTS

All link components, related expressions and optimizations were modeled with Matlab. Power and area of the link were computed for 130nm and 70nm technologies and for various wire width factors (×1-×10) versus length (with constant T_{serial}=16Gbps) and throughput (with constant L=1.5cm). The Berkeley parameter extraction tool (BPTM) [21]~~[21]~~ was used to predict parameters of the 70nm process for both interconnects and devices using BSIM3v3 models. These parameters were combined with estimates of the ITRS [17]~~[17]~~ and were verified using SPICE [12]~~[12]~~. Simulations were conducted for two types of parallel links, multi-layer and single-layer structures. The obtained parameters of repeaters varied with respect to wire lengths and widths from 1 to 3 devices with scaling factors of 31 to 316 in the serial link.

The 32-bit serializer was assumed to have asynchronous control [7]~~[7]~~, using a critical path of six NAND gates [8]~~[8]~~. The total count of logical gates in the serializer with the asynchronous control was assumed to be 500 (accounting for the increased number of gates in asynchrounous circuits). Similar assumptions were made for the deserializer.

A Multi-Layer Parallel Link **-** The number of repeaters varied from 1 to 8 with scaling factors of 9 to 47 with respect to different wire lengths and widths. As can be seen in Figure 2~~Figure 2~~ and Figure 3~~Figure 3~~, there are "break-even" points of length beyond which the serial link (solid line) dissipates lower power – 400-2000um in 130nm as compared to 170-600um for 70nm. The relative benefit in 70nm is more pronounced than in 130nm – up-to ×5.5 and ×3.7, respectively, due to increased leakage current of the repeaters and drivers in the parallel link. Figure 4~~Figure 4~~ shows reduction of area of up-to ×17 in the serial link in 70nm (68000µm^2 vs. 4200µm^2), with "break-even" point for shortest narrow wires because of the dominating area of the serializer.

As can be seen in Figure 5~~Figure 5~~, beyond a certain throughput level, the parallel design in 70nm consumes lower power due to transistor scaling in the serializer for reduced circuit delay. The "break-even" in 70nm is at 40Gbps for minimal width wires. Drastic reduction of the area ratio in Figure 6~~Figure 6~~ at high throughput values is also caused by scaling of the serializer.

Single-Layer Parallel Link **–** The number of repeaters varied from 1 to 3 with scaling factors of 4 to 224. As is evident in Figure 7~~Figure 7~~, the parallel link consumes lower power thanks to reduced wire capacitance and reduced scaling factors and count of repeaters. However, this arrangement results in extremely high area, leading to ×65 ratio between the parallel and serial links.

V. SUMMARY AND FUTURE WORK

The comparative analysis of interconnects in NoC revealed significant improvements of up to ×5.5 and ×17 in power and area consumptions in serial links as compared to parallel links. The main source of this improvement is the low number of wires and repeaters needed for the serial link. Results obtained for 130nm and 70nm technologies show increasing ratio of improvement due to higher leakage currents in advanced sub-micron technologies. Two parallel link structures, multi-layer and single-layer, were used as reference; the single-layer link showed better results in terms of power but was dramatically (×65) larger in area.

Future research may consider various levels of serialization, as well as application of wire-pipelining in order to speed up the serial link and to investigate other potential advantages of the technique. Additional factors as noise and crosstalk should be considered and analyzed in future investigations.

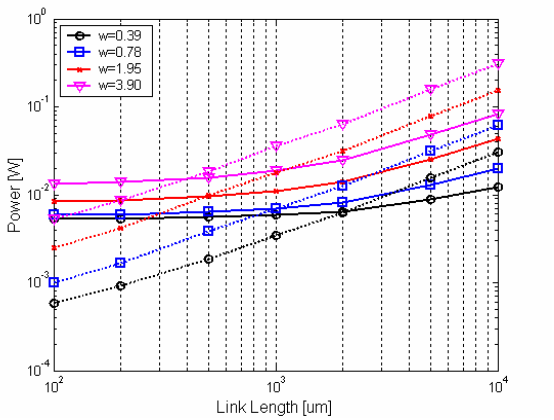

Figure 2. *Power in serial and parallel links (130nm, multi-layer)*

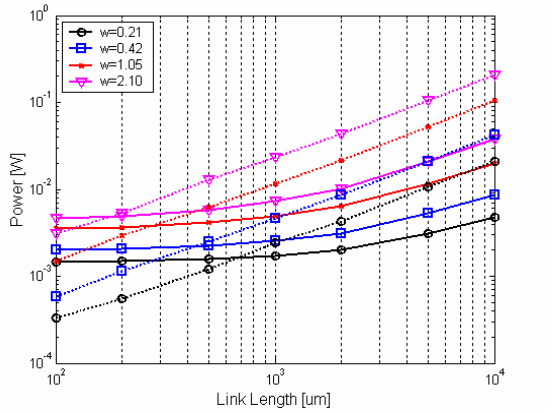

Figure 3. *Power in serial and parallel links (70nm, multi-layer)*

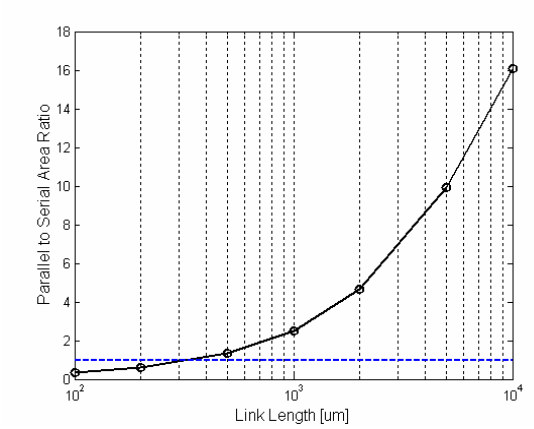

Figure 4. *Ratio of area vs. link length (70nm, multi-layer)*

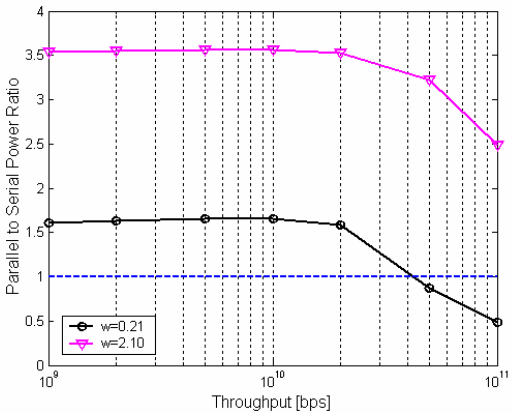

Figure 5. *Ratio of power vs. throughput (70nm, multi-layer)*

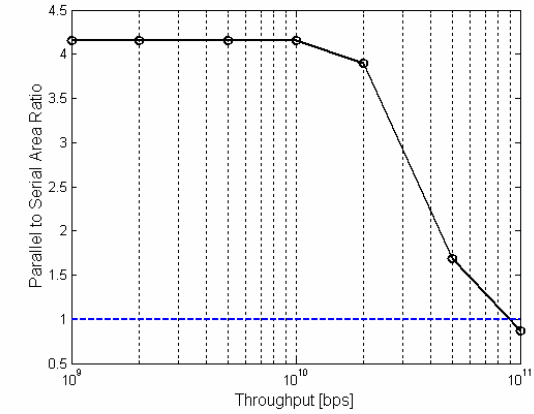

Figure 6. *Ratio of area vs. throughput (70nm, multi-layer)*

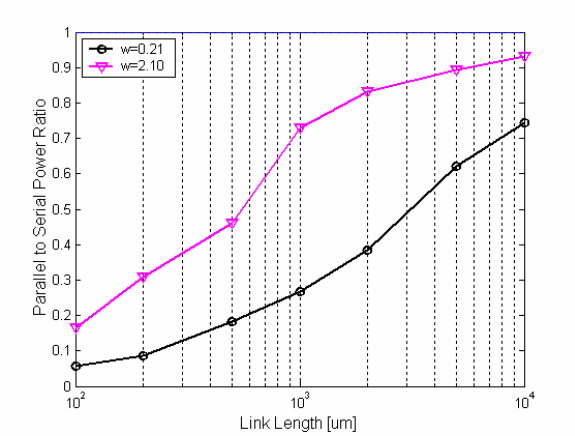

Figure 7. *Ratio of power vs. link length (70nm, single-layer)*

VI. ACKNOWLEDGEMENTS

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