Automated Measurement and Analysis of MIS Interfaces in Narrow-Bandgap Semiconductors

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Abstract—A computerized system for simultaneous measurement of high-frequency and quasi-static MIS capacitance is described. The importance of this simultaneity in the application of various analysis methods to MIS devices in narrow-bandgap semiconductors is discussed. Results on the interfaces of mercury-cadmium-telluride with zinc sulfide and anodic oxide are given.

INTRODUCTION

MEASUREMENT of the capacitance dependence on the voltage (C-V) in Metal-Insulator-Semiconductor (MIS) structures, is one of the methods most widely used to study the properties of the semiconductor interface [1]-[7]. This paper is concerned in MIS C-V surface characterization of narrow-bandgap materials such as $Hg_{1-x}Cd_xTe$ and InSb. The application of C-V analysis to these semiconductors is more complicated than to the Si-SiO_2 system, where most of the earlier work had been performed. In addition to problems such as interface traps and surface nonuniformity, C-V curves in InSb and $Hg_{1-x}Cd_xTe$ are characterized by hysteresis [8], [9], which complicates measurement and interpretation. Furthermore, due to their energy-bands structure, these materials become degenerate at moderate electron concentrations, so that the usual Maxwell-Boltzmann approximation is inaccurate in calculation of theoretical curves. Fermi-Dirac statistics must be used, and the nonparabolic behavior of the bands may be approximated by the Kane model [1], [4], [10]-[12]. When a degenerate accumulation layer of electrons is present near the surface of an n-type material, its surface concentration is limited according to Fermi-Dirac statistics, in contrast with the Maxwell-Boltzmann approximation which allows the surface charge concentration to grow exponentially towards infinity. Thus the width of the accumulation layer is larger than that calaculated by the Maxwell-Boltzmann approximation, and its associated capacitance is smaller. If neglected, this effect would lead to a large apparent interface trap density.

A computer-controlled measurement system has been developed, capable of measuring simultaneously the small-signal capacitance at 1 MHz and at very low frequency (quasi-static measurement). The simultaneous measurement is a very useful method to overcome some of the difficulties in interpretation of C-V curves which exhibit hysteresis, as will be shown below. Furthermore, it provides criteria for checking the lateral uniformity of the MIS device. The system can also perform data analysis by various methods, for determining bulk and interface parameters. The combination of measurement, data acquisition, computing capabilities and graphic display yields accuracy and efficiency that are difficult to achieve by graphical analysis of C-V plots.

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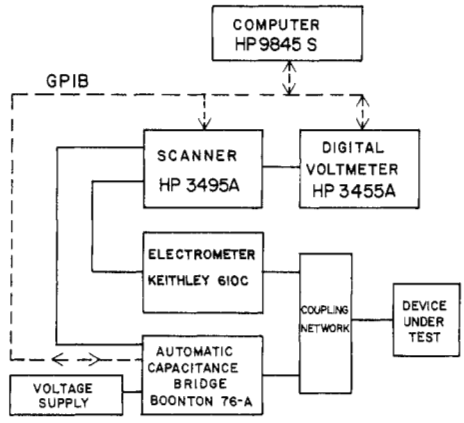

Fig. 1. A block diagram of the experimental system, which is capable of measuring simultaneously the high-frequency and quasi-static capacitance.

EXPERIMENTAL

A block diagram of the experimental system is shown in Fig. 1. The high-frequency (1-MHz) small-signal capacitance (C_{hf}) and conductance (G_{hf}) are measured with an automatic capacitance bridge (Boonton 76 A). This instrument includes a 1-MHz test-voltage source with adjustable amplitude from 5 to 150 mV, and a programmable dc voltage supply which is used to change the bias voltage on the MIS capacitor in small steps. An external voltage supply is required to extend the bias range to negative values. The amount of stored charge (Q) in the MIS capacitor at each bias voltage is measured by an electrometer (Keithley 610-C). The quasi-static capacitance (C_{lf}) is the voltage derivative of the stored charge. The automatic capacitance bridge is controlled directly by a desktop computer (HP 9845S) via GPIB (IEEE Standard 488). The bias voltage and the electrometer analog output are sampled by a GPIB-controlled voltmeter and a scanner. The device under test is in our case an MIS capacitor made on a narrow-bandgap semiconductor. It is mounted in a dewar cooled to liquid-nitrogen temperature, at which the narrow-bandgap semiconductor is extrinsic. The device is cold shielded from background radiation in order to prevent optical generation of

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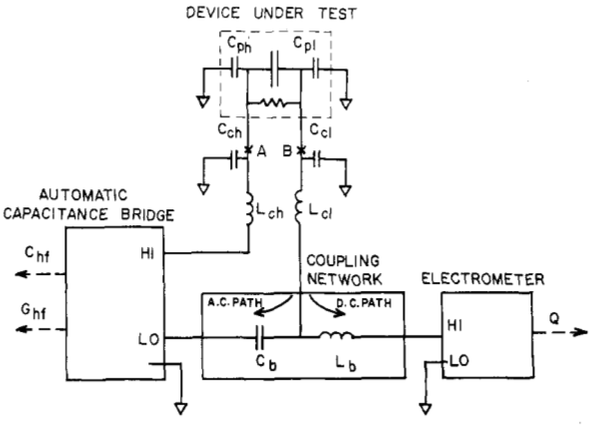

Fig. 2. Schematic description of the measurement circuit, showing the coupling network and the parasitic elements. C_{ch} and C_{ph} have no effect, since the bridge performs a three-terminal measurement. The admittance between the low side of the DUT and the ground (C_{cl}, C_{pl}, and L_b in series with the electrometer input admittance) must be used to correct the bridge readings.

electron-hole pairs in the semiconductor; thus one may assume that the device is in thermal equilibrium.

The novel feature of this experimental setup is the simultaneous measurement of high-frequency and quasi-static capacitances, which is important for accurate data analysis. This is accomplished by separating the dc and ac paths with a simple coupling network consisting of a capacitor (C_b) and an inductor (L_b), as illustrated in Fig. 2.

The measured data should be corrected in order to compensate for the effects of the coupling network, parasitic impedances, and dc leakage. The correction procedures are described in Appendix A. The accuracy of both high-frequency and quasi-static capacitance measured by this setup was checked using standard capacitors and was found to be better than 0.5 percent.

Analysis Methods

A. Basic Semiconductor and Device Parameters

Some external parameters are required in order to analyze the measured data. These are the semiconductor's dielectric constant ϵ_s, the bandgap E_g, effective densities of states N_c, and N_v, the temperature T, and the capacitor area A. For Maxwell-Boltzmann statistics the intrinsic concentration n_i is sufficient (instead of E_g, N_c, and N_v). The impurity concentration in the crystal N_b may be found by iterative fitting of the theoretical high-frequency capacitance minimum in equilibrium inversion $C_{\min}$ to the measured value. N_b is used to compute the location of the bulk Fermi level and the flatband capacitance C_{fb}, which defines the measured flatband voltage V_{fb}. This voltage depends on interface parameters (using a new standard terminology [13])

$$V_{fb} = \phi_{ms} - \frac{q(N_f + N_m + N_{ot})}{C_{ox}/A} + \frac{qN_{it}(0)}{C_{ox}/A} \tag{1}$$

where ϕ_{ms} is the metal-semiconductor work-function difference, N_f, N_m, and N_{ot} represent surface densities of fixed, mobile, and trapped charges in the insulator, and $N_{it}(0)$ is the number of interface traps (states) occupied by electrons when the surface potential ϕ_s is zero. In elementary analysis all these terms may be grouped to an effective surface charge, commonly referred to as Q_{ss}. Individual characterization of these parameters is the purpose of the following analysis methods.

B. Determination of the Surface Potential

Calculation of the surface potential and its dependence on the gate voltage V is an essential step in the analysis; the presence of surface states should not affect this calculation. However, in different voltage sweeps this dependence may be changed due to hysteresis in the C-V curve. The simultaneous measurement of high-frequency differential capacitance C_{hf} and total charge Q allows calculation of the surface potential in two independent ways. The quasi-static method, which is equivalent to Berglund's graphical integration [3] is based on

$$V - V_{fb} = \phi_s + V_{ox} = \phi_s + \frac{Q}{C_{ox}}. \tag{2}$$

The additive constant V_{fb} may be found from the high-frequency measurement as described above. The high-frequency method for finding ϕ_s is based on numerical inversion of the theoretical formula

$$C_{hf}(\phi_s) = f(\phi_s, E_g, N_c, N_v, T, \epsilon_s, A, C_{ox}, N_b) \tag{3}$$

for every measured value of C_{hf}. Both methods should yield the same dependence $\phi_s(V)$ for a uniform sample, even in the presence of hysteresis. However, some limitations should be mentioned: the high-frequency method is sensitive to the external parameter values in (3), and it cannot resolve surface potentials above the onset of strong inversion [14]. Furthermore, it depends on the assumption that no surface-charges follow the small high-frequency component of ϕ_s. The quasi-static method is more direct, but it is very sensitive to errors in the value of C_{ox}, and to nonequilibrium conditions (such as incident photon radiation). Unstable leakage through the insulator may affect the accuracy of the measured capacitor charge.

C. Hysteresis Analysis

Long-term trapping effects cause hysteresis in the C-V curves, as shown in Fig. 3. The direction of the hysteresis loop indicates whether the trapped charges are injected from the semiconductor or move in the insulator towards the interface. Quantitative characterization of the hysteresis charge is made possible by our simultaneous measurements of high-frequency and quasi-static capacitances. Consider the points A and B in Fig. 3 which correspond to the same high-frequency capacitance (and thus to the same ϕ_s and same semiconductor charge Q_s). The voltage shift ΔV_{AB} results from trapping of charge ΔQ_{AB}, which is measured by the electrometer. If this charge is injected from the bulk and trapped at the interface, then $\Delta Q_{AB}/\Delta V_{AB} = C_{ox}$. However, if the charge is trapped in the insulator at an average distance $\bar{x}$ from the gate, then

$$\frac{\bar{x}}{t_{ox}} = C_{ox}\frac{\Delta V_{AB}}{\Delta Q_{AB}} \leqslant 1 \tag{4}$$

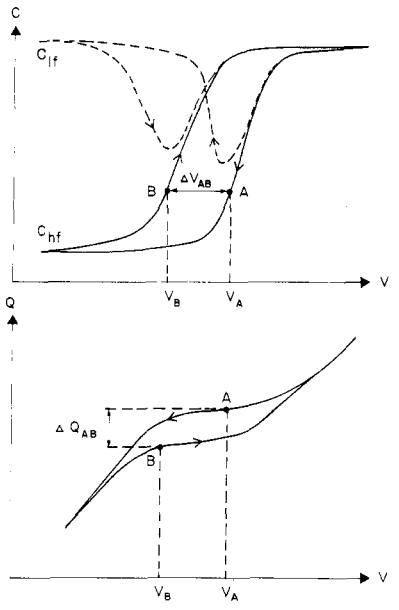

Fig. 3. Schematic dependence of differential capacitance and stored charge on bias voltage in an MIS capacitor exhibiting injection-type hysteresis.

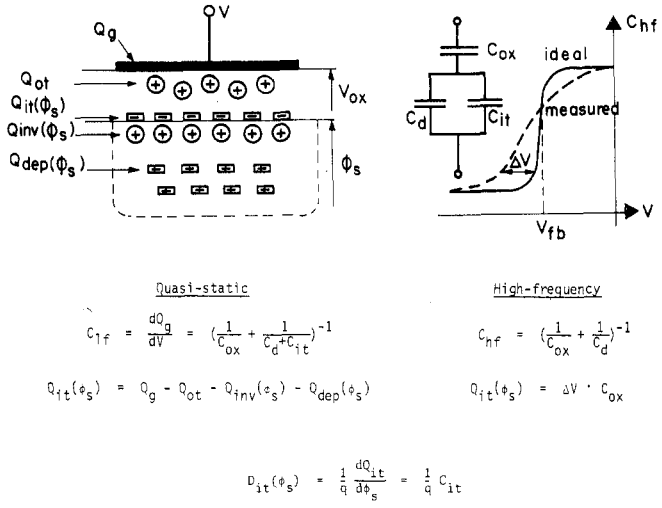

Fig. 4. Comparison of the methods for calculating interface-trap densities.

where t_{ox} is the insulator thickness. The charge-centroid $\bar{x}$ has been measured in a similar manner in silicon nitride, from the shift in flatband voltage [15]. In many cases, the hysteretic C-V curves are not parallel, indicating that trapping and detrapping take place also during the transition between accumulation and inversion. In such cases, these processes cannot be separated from fast interface trapping, but the variations in total trapped charge and its centroid may still be determined.

D. Interface Trap Distribution $D_{it}(\phi_s)$

Two methods for calculation of interface trap (state) distribution are illustrated in Fig. 4. These methods are equivalent to the quasi-static method [5], [6], and the differentiation method [2]. In both methods, every deviation of the measured data from the ideal theoretical values is attributed to interface traps distributed across the energy gap. The two methods rely on the previously calculated surface potential $\phi_s(V)$ and assume that the charge of the interface traps depends only on ϕ_s. According to the quasi-static method, the interface-trapped charge is

$$Q_{it}(\phi_s)\ [\mathrm{C \cdot cm^{-2}}] = Q_{\mathrm{measured}} - Q_{ot} - Q_{\mathrm{ideal}}(\phi_s) \tag{5}$$

and the energy distribution of traps is found by numerical differentiation assuming a step-function approximation to the Fermi probability function

$$D_{it}(\phi_s)\ [\mathrm{eV^{-1} \cdot cm^{-2}}] = \frac{dN_{it}(\phi_s)}{d\phi_s} = \frac{1}{q}\frac{dQ_{it}(\phi_s)}{d\phi_s}. \tag{6}$$

In the high-frequency method, the extra voltage drop on the insulator, caused by the trapped charge, is used to calculate

$$Q_{it}(\phi_s) = [(V - V_{fb}) - V_{\mathrm{ideal}}(\phi_s)] \cdot C_{ox} \tag{7}$$

and the energy distribution $D_{it}(\phi_s)$ is found by (6).

In fact, the direct attribution of trapped charge to the surface potential is not always justified, as mentioned before. A charge Q trapped at a distance $\bar{x}$ from the metal gate is sensed by the high-frequency method as an effective charge $\bar{x}/t_{ox} \cdot Q$ at the interface, while the quasi-static method is insensitive to the location $\bar{x}$. The main drawback of these methods is that a lateral nonuniformity in the device is interpreted as apparent interface-traps distributions [16].

For a laterally-nonuniform device, there is a discrepancy between the surface potentials calculated by the quasi-static method and by the high-frequency method. Such devices should not be analyzed by reference to one-dimensional theory. Since C_{lf} and C_{hf} should coincide in depletion and accumulation if there are no surface traps, an estimate of the interface trap density can be obtained for a nonuniform device by calculating $C_{it} = qA \cdot D_{it}$ from the difference between C_{lf} and C_{hf} in these regimes (see the equivalent circuit in Fig. 4). Since the capacitances are measured simultaneously, this difference can be determined reliably even in the presence of hysteresis.

Results

This section demonstrates the application of the methods described above to MIS structures made on $Hg_{1-x}Cd_xTe$. This semiconductor is a ternary compound useful for infrared applications [17]. For the composition $x = 0.26$, its energy gap is about 0.19 eV at 77 K, and the electron effective mass is about 0.015 m_0 at the conduction band edge. The experimental devices were made on randomly oriented wafers from crystals grown by solid-state recrystallization.

The wafers were mechanically polished with 0.3-μm Al_2O_3 and etched in 10-percent bromine in methanol. A 1-μm-thick layer of ZnS was initially evaporated on the wafers, and then windows were etched in the ZnS. Native oxide films were grown by anodic oxidation in 0.1M KOH in 90-percent ethylene glycol + 10-percent H_2O [18]. In some samples, a thin layer of evaporated ZnS was used instead of the oxide. Indium gate electrodes were then evaporated on the thin insulator, with bonding pads on the thick ZnS. The pad capacitance was

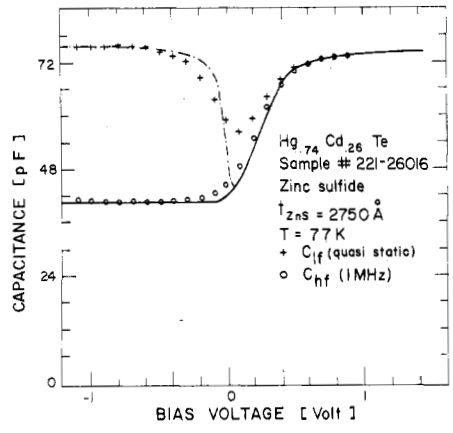

Fig. 5. Measured and theoretical C-V curves for a $Hg_{0.74}Cd_{0.26}Te$ capacitor with ZnS insulator. Data points, measured simultaneously at high and low frequencies, are indicated by symbols. Continuous lines represent theoretical curves calculated using Fermi-Dirac statistics and Kane's band model. The theoretical curves are based on the following parameter values: $C_{ox} = 76.5 \times 10^{-12}$ F, $A = 3.2 \times 10^{-3}$ cm^2, $T = 77$ K, $N_b = 7.4 \times 10^{14}$ cm^{-3}, $V_{fb} = 0.39$ V, $Q_{ss} = -5.85 \times 10^{10}$ cm^{-2}, $E_g = 0.188$ eV, $n_i = 8.25 \times 10^{10}$ cm^{-3}, $m_e^*(0) = 0.015\ m_0$, $m_h^* = 0.7\ m_0$, $\epsilon_s = 18$.

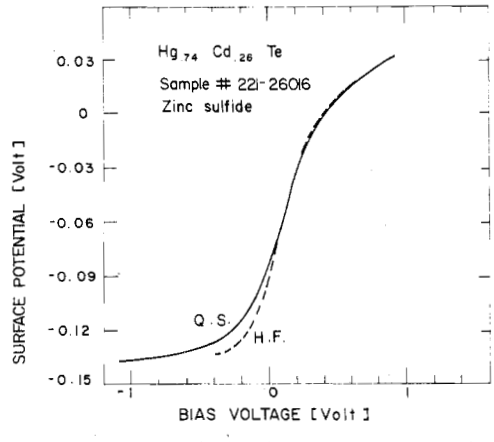

Fig. 6. Surface potentials calculated from the measured quasi-static (Q.S.) and high-frequency (H.F.) capacitances shown in Fig. 5.

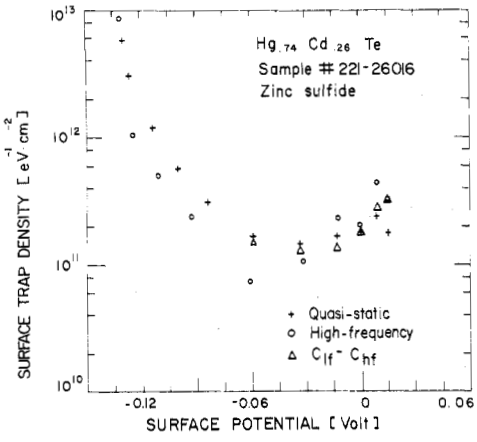

Fig. 7. Interface trap density calculated for the device of Fig. 5 by the high-frequency method, the quasi-static method and from the differences between C_{hf} and C_{lf}.

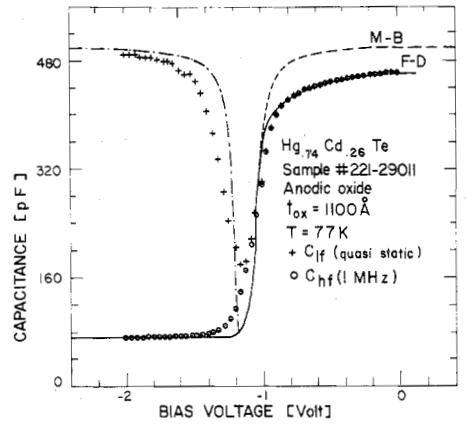

Fig. 8. Measured and theoretical C-V curves for a $Hg_{0.74}Cd_{0.26}Te$ capacitor with anodic oxide insulator. Data points are indicated by symbols. Continuous lines represent theoretical curves calculated using Fermi-Dirac statistics (F-D) with Kane's band model, and Maxwell-Boltzmann statistics (M-B) assuming parabolic bands. The theoretical curves are based on the following parameter values: $C_{ox} = 5.05 \times 10^{-10}$ A, $A = 3.2 \times 10^{-3}$ cm^2, $T = 77$ K, $N_b = 7 \times 10^{14}$ cm^{-3}, $V_{fb} = -1.04$ V, $Q_{ss} = 1.02 \times 10^{12}$ cm^{-2}, $E_g = 0.188$ eV, $n_i = 8.25 \times 10^{10}$ cm^{-3}, $m_e^*(0) = 0.015\ m_0$, $m_h^* = 0.7\ m_0$, $\epsilon_s = 18$.

at most 2 percent of the total capacitance, and was subtracted prior to analysis. The contact to the bulk was made by evaporating indium on the back side of the wafer, and the devices were bonded in flatpacks. It was observed that good ohmic contacts are important for accurate measurements [16].

Fig. 5 shows the experimental data measured on a capacitor having ZnS as gate insulator. The basic device parameters were found from the high-frequency capacitance, and the theoretical ideal curves were calculated, using Fermi-Dirac statistics, and plotted on the same figure. The surface potential was computed from the measured C-V data by the two methods described in the preceding section.

Results are shown in Fig. 6, exhibiting a reasonable fit between the two methods. The slight differences indicate some nonuniformity in the insulator thickness or insulator charge. In strong inversion only the low-frequency method is applicable. The deviations of the measured points from the ideal curves in Fig. 5 are intepreted in terms of surface-trap densities, calculated by the methods presented above, and are plotted for comparison in Fig. 7. It should be noted that the calculated interface-trap densities in strong accumulation and inversion suffer from large inaccuracy. The reason for this inaccuracy becomes evident if (6) is written in the form

$$D_{it}(\phi_s) = \frac{1}{q} \frac{dQ_{it}}{dV} \cdot \frac{dV}{d\phi_s} . \tag{8}$$

Since $dV/d\phi_s \to \infty$ in accumulation and inversion, the measured quantity dQ_{it}/dV must be very small and it is very difficult to measure. The surface trap density near midgap is about 10^{11} cm$^{-2} \cdot$ eV^{-1} for this sample.

Fig. 8 shows experimental results measured on a $Hg_{0.74}Cd_{0.26}Te$ capacitor having native oxide as an insulator, along with the theoretical curves. The ideal curves calculated using both Maxwell-Boltzmann and Fermi-Dirac statistics are shown for comparison, and it is evident that the effect of

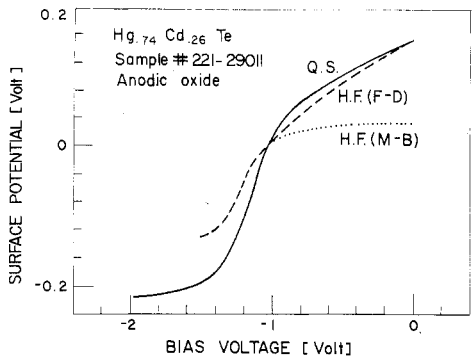

Fig. 9. Surface potentials calculated from the measured quasi-static (Q.S.) and high-frequency (H.F.) capacitances shown in Fig. 8. Lateral nonuniformity is indicated by the differences between Q.S. and H.F. The calculation based on high-frequency capacitance was made using Fermi-Dirac statistics (F-D) and Maxwell-Boltzmann statistics (M-B).

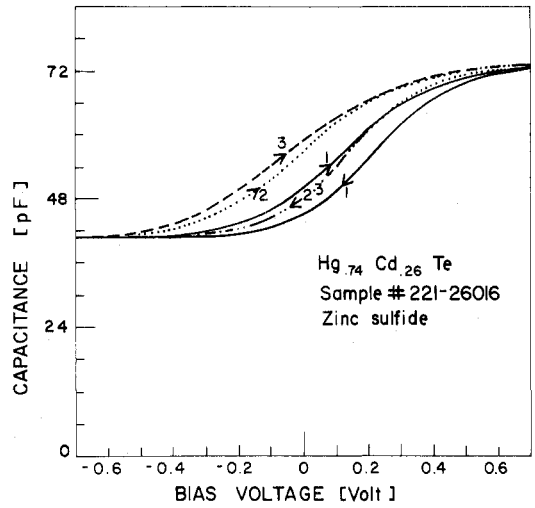

Fig. 10. Hysteresis curves of the capacitor of Fig. 5 for bias sweep ranges (-1, 1), (-1.5, 1.5), and (-2, 2) V. The shift in the negative direction indicates hole trapping.

degeneracy in accumulation is important. The measured MIS capacitance in accumulation clearly follows the Fermi-Dirac theory. The measured high frequency and quasi-static capacitances are almost equal in depletion and accumulation, but their slope is slightly smaller than the theoretical. In addition, it was impossible to fit the surface potential calculated by the two methods from the experimental data. This is an indication of nonuniformity in the device [19], [20]. This point is illustrated in Fig. 9, which shows also the effect of degeneracy on the calculated surface potential. Ignoring this nonuniformity, an apparent surface trap density of above 3×10^{11} $cm^{-2} \cdot eV^{-1}$ would be extracted from the C-V curves. The true interface-trap density in the device may be estimated by comparing the high- and low-frequency capacitances at the same voltage in the depletion and accumulation regimes. Such a comparison is enabled by the simultaneous nature of the measurement. For the device in Fig. 8, $D_{it} \simeq 3 \times 10^{10}$ $cm^{-2} \cdot eV^{-1}$.

The interface of the anodic oxide with $Hg_{1-x}Cd_xTe$ and the ZnS interface may be compared also in terms of hysteresis. As can be seen in Fig. 10, ZnS exhibits injection-type hysteresis which is proportional to the sweep amplitude, and the flat-band voltage shift is almost entirely in the negative direction, indicating hole trapping. We have observed that the anodic oxide interface is characterized by a smaller hysteresis of the same type, which is reduced after the application of a few voltage sweeps at 77 K [9]. The centroid of trapped charge in these devices was very close to unity. The variation of slopes in the curves of Fig. 10, indicates that at least some of the traps of Fig. 7 are related to hysteresis and do not depend only on surface potential.

InSb MIS capacitors with native anodic oxide of about 700 Å have also been studied. Typically, these capacitors exhibited large hysteresis with charge centroid of about 0.8. The interface-trap density (if attributed directly to surface potential) was above 5×10^{11} $cm^{-2} \cdot eV^{-1}$.

Our results show that the $Hg_{1-x}Cd_xTe$ anodic oxide interface has an exceptionally low trap density, compared to previous C-V measurements in compound semiconductors [1], [19]-[23]. Indirect estimates, based on charge transfer efficiency achieved in $Hg_{1-x}Cd_xTe$ CCD's using a similar interface [9], [19], correspond to approximately the same trap density. However, the slow trapping, expressed by hysteresis in the C-V curves, might be disadvantageous for MIS devices, e.g., threshold-voltage instability in MIS transistors [21]. The large value of fixed oxide charge ($Q_{ss} \simeq 10^{12}$ cm^{-2}) may cause additional difficulties.

In comparison with the two other interfaces studied, InSb-anodic oxide and $Hg_{1-x}Cd_xTe$-ZnS, $Hg_{1-x}Cd_xTe$-anodic oxide is the most promising for narrow-bandgap MIS device applications.

Conclusions

The system described above is an efficient tool for characterization of MIS interfaces. Although narrow-gap materials have been emphasized in the discussion, the system is applicable to any MIS interface. The system can be extended by adding measurements of the small-signal admittance at intermediate frequencies. From such measurements the time-constants of energy-loss processes may be determined. Complementary information about the interface-trap density can be extracted from the dependence of the conductance on frequency [7]. However, the principal energy-loss process in some materials may be depletion-region generation-recombination [19] or insulator leakage, rather than charging-discharging of interface traps.

The information obtained from a C-V experiment can be used to evaluate technological processes in which MIS structures are made, such as CCD's and MIS transistors. Although direct interpretation in terms of the device performance is difficult [19]-[21], the simplicity of sample preparation and the ease of the automated measurement make this technique useful and convenient.

Appendix A
Correction Procedure for the Measured Capacitances

The high-frequency bridge readings must be corrected for the effects of the capacitance C_b and the cable inductances $L_{ch} + L_{cl}$ (see Fig. 2). In addition, the effects of parasitic impedances to ground must be considered. Those impedances

which are tied directly to the bridge ports have no effect, since this is a three-terminal Young bridge. However, the impedances between the low side of the DUT and the ground (C_{cl}, C_{pl}, and L_b in series with the electrometer input admittance) provide a parasitic path to ground besides the principal ac path through C_b. The true impedance of the DUT can be calculated from the expression

$$Z_{\text{DUT}} = (Z_{\text{measured}} - Z_b)\left(\frac{Z_p}{Z_p + Z_b}\right) - j\omega L_{\text{cable}} \tag{9}$$

where Z_b is the impedance of C_b, Z_p is the parasitic impedance between the low side of the DUT and the ground, and L_{cable} is the cable inductance (assuming it consists only of L_{ch}). These parameters are determined by a setup procedure as follows:

1) Z_b is measured by connecting C_b directly to the bridge terminals;
2) A reference capacitor is measured directly on the bridge terminals, and then remeasured in place of the DUT (using the cables without the coupling network and the electrometer). L_{cable} is determined from the difference in the measured impedances;
3) The measurements circuit is set as in Fig. 2, and the known reference capacitor is measured between points A and B. The DUT is disconnected from point A only. Equation (9) is then solved for Z_p. C_{ph} is designed to be negligible in order for this procedure to be exact.

In our measurements we have chosen C_b of the order of C_{ox}. Z_p was mainly capacitive, corresponding to $C_p \simeq 20$ pF. L_{cable} was typically 0.3 μH, L_{cl} was less than 0.1 μH. The DUT was packaged in such manner that C_{ph} was less than 0.5 pF.

DC leakage in the DUT or the cables, or a drift in the electrometer can cause a change of Q that is time dependent rather than voltage dependent. To compensate for this effect, the electrometer output is sampled twice at each voltage. The measurements are equally spaced in time, and bias steps are applied after every second measurement. Any difference ΔQ between the charge readings at the same voltage are attributed to leakage and drift currents. These currents are assumed to be constant in time for each voltage, and their cummulative effect is subtracted using the expression

$$Q_{\text{DUT}} = Q_{\text{measured}} - 2\Sigma\Delta Q. \tag{10}$$

Thus only capacitively stored charge is considered. The typical correction in our experiments corresponded to a leakage of a few picoampers.

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