tion for $M = 512$. Note that if the criteria of (5)-(7) are satisfied, the area change ΔQ and surface concentration error are less than 2 percent.

The calculations were performed on a System 370/Model 168 computer using the APL.SV programming language. Calculation time for $M = 256$ was typically 0.8 s. Trials with finite difference methods indicate about a 50-s computation time, showing the efficiency of the method.

Thus we have shown that FFT methods can simulate this semiconductor process. The process can be applied to general profiles, and the error incurred for reasonable numbers of points is adequately small for engineering-type calculations.

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Diffusion Profiling Using the Graded $C(V)$ Method

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Abstract—**A simple and quick technique for determination of impurity-diffusion profiles in semiconductors from MOS $C(V)$ measurements on a gradually etched surface is presented and analyzed. This technique is most useful for slowly varying profiles in the range of 10^{16}-5×10^{18} cm^{-3}. Experimental profiles are given for P in Si, and for Cd in InSb.**

INTRODUCTION

Evaluation of diffused profiles [1]-[3] usually involve the tedious task of removing successive thin layers between measurements. The electrical profiling techniques based on sheet resistivity and Hall effect are further complicated by contact problems and mobility variations. This work presents a simple method for obtaining diffusion profiles of electrically active impurities in a semiconductor from a series of $C(V)$ measurements on MOS capacitors. It eliminates the necessity for repetitive sample processing, and is easy in terms of data analysis. The method is based on gradual immersion of a long diffused sample in an etching solution so that the surface becomes a slightly sloped plane, along which the impurity concentration is gradually changing. MOS capacitors are fabricated on the etched surface by depositing an insulating layer with small metal electrodes upon it, as shown schematically in Fig. 1. The impurity concentration underneath each capacitor may be deduced from the ratio of minimum to maximum capacitance in its $C(V)$ curve [4]. The detailed $C(V)$ dependence is not significant, in contrast to similar capacitance methods which involve numerical differentiation of the measured curve [5]. Combining the concentration data with the local etching depth for each capacitor gives the diffusion profile.

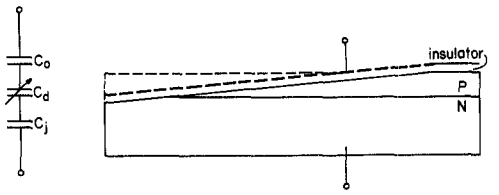

Fig. 1. Schematic cross section of a diffused sample after gradual etching and capacitor fabrication. Also shown is the capacitance model.

ANALYSIS

The capacitance measured at high frequency (Fig. 1) can be represented by three capacitors in series:[1]

1) the insulator capacitance C_o
2) the depletion-region capacitance
3) the p-n junction capacitance C_j.

Since the junction area is much larger than the metal area, C_j may be neglected in series with the two others, and the measured capacitance is

$$C = \left(\frac{1}{C_o} + \frac{1}{C_d}\right)^{-1} = \left(\frac{x_o}{\epsilon_i \cdot \epsilon_o \cdot A} + \frac{x_d}{\epsilon_s \epsilon_o A}\right)^{-1} \quad (1)$$

where A is the metal-gate area, ϵ_i and ϵ_s are the dielectric constants of the insulator and the semiconductor, respectively, x_o is the insulator thickness, and x_d is the depletion-region width.

The maximum value of C (measured at voltages that cause surface accumulation) is simply C_o. The minimum measured capacitance corresponds to the depletion region of maximum width x_{dm}, which may be calculated from measured data using the expression

$$x_{dm} = \epsilon_s \epsilon_o \left(\frac{A}{C_o}\right)\left[\frac{1 - \frac{C_{\min}}{C_o}}{\frac{C_{\min}}{C_o}}\right]. \quad (2)$$

Let us assume at this point that the impurity concentration N is constant throughout the depletion region. By solving Poisson's equation using the depletion approximation we can

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[1] This model is valid as long as the depletion region edge does not reach the junction.

relate x_{dm} to the semiconductor parameters [6], provided that C_{min} is measured in a steady state at high frequency. By equating expressions for x_{dm} we obtain

$$\frac{N}{\frac{k_B T}{q}\ln\left(\frac{N}{n_i}\right)} = \frac{4}{q\,\epsilon_s \cdot \epsilon_o}\cdot\left(\frac{C_o}{A}\right)^2\left[\frac{\frac{C_{min}}{C_o}}{1-\frac{C_{min}}{C_o}}\right]^2 \tag{3}$$

from which N may be computed using experimental data. k_B is Boltzmann's constant, q is the electron charge, T is the semiconductor temperature, and n_i is the intrinsic carrier concentration of the semiconductor at temperature T.

Let us examine the principal error sources in order to determine the accuracy of the method and its limitations. The error sources are:

1) *Variation in impurity concentration in the depletion region:* The diffused impurity concentration in the depletion region is not constant, but rather decreasing with increasing depth, so that x_{dm} obeys the integral form of Poisson's equation

$$\phi_s = 2\phi_F = \frac{q}{\epsilon_o \epsilon_s}\int_0^{x_{dm}}\int_0^{\xi} N(x)\,dx\,d\xi \tag{4}$$

assuming that the surface potential ϕ_s is equal to twice the Fermi potential ϕ_F when the depletion region reaches its maximum width [6]. $N(0)$ may be calculated from x_{dm} only if the form of the function $N(x)$ is known. By the mean value theorem it may be shown that applying (3) in this case leads to a value N which corresponds to some intermediate depth $\bar{x}$ in the depletion region. Hence, it is convenient to present the result N as an exact value, with some uncertainty Δx_1 about its location. An upper bound for Δx_1 is the total depletion region width x_{dm}, as given by (2). Except for low-doping levels, Δx_1 is very small. For example, in silicon at room temperature with impurity concentration above 5×10^{16} cm^{-3}, Δx_1 is less than 0.15 μm. It should also be noted that in capacitors located near the p-n junction x_{dm} may reach the junction plane. The measured capacitances then resemble low-frequency $C(V)$ behavior due to minority-carrier supply from the bulk, and cannot be used for evaluating N.

2) *Gradual change in impurity concentration under the metal electrode caused by the surface slope:* This may be represented by an additional error term Δx_2 which may be estimated as the product of surface slope and capacitor width. To reduce Δx_2, a moderate slope should be made on a long sample together with relatively small capacitors' dimension in the slope's direction.

3) *Inaccuracy in etching depth measurement and nonuniform etching* contribute a third error element Δx_3.

4) *Capacitance measurement errors:* Note that at high-impurity concentration the value of C_{min}/C_o is very close to unity, and small errors in measuring the capacitance cause large errors in the calculated N. The minimum detectable difference in capacitance determines the maximum measurable impurity concentration.

5) *Parasitic effects* such as photogeneration of carriers or fast surface states may cause deterioration of the $C(V)$ curve. These effects tend to appear as capacitances in parallel to C_d, causing the calculated value to be an overestimate of N.

Experimental

The graded $C(V)$ technique presented previously has been employed for measuring diffusion profiles of phosphorus in silicon, and of cadmium in indium antimonide.

Indium antimonide samples were ⟨111⟩ oriented tellurium-doped p-type wafers with impurity concentration of about 10^{15} cm^{-3}. Cadmium diffusion was performed at 400°C for 6.5 h in a closed ampoule. After the diffusion, a slice about 2.5 cm long was gradually immersed and etched in a solution of lactic acid, HNO_3, and Hf, so that a height difference of about 2 μm was obtained. A narrow strip along the sample had been protected by photoresist before the etching, so that a step was formed, and the distance from every point on the wedged surface to the original surface could be determined by a direct measurement of the step height. A 1000-Å pyrolitic SiO_2 layer was then deposited on the sample, and a series of 0.6-mm diameter capacitors were formed on it by Cr–Au evaporation. $C(V)$ curves of these capacitors at 1 MHz were measured by probing the sample at 77 K. The shape of the C–V curves indicate that the surface-state density is low enough so that their effect on C_{min}/C_o can indeed be neglected.

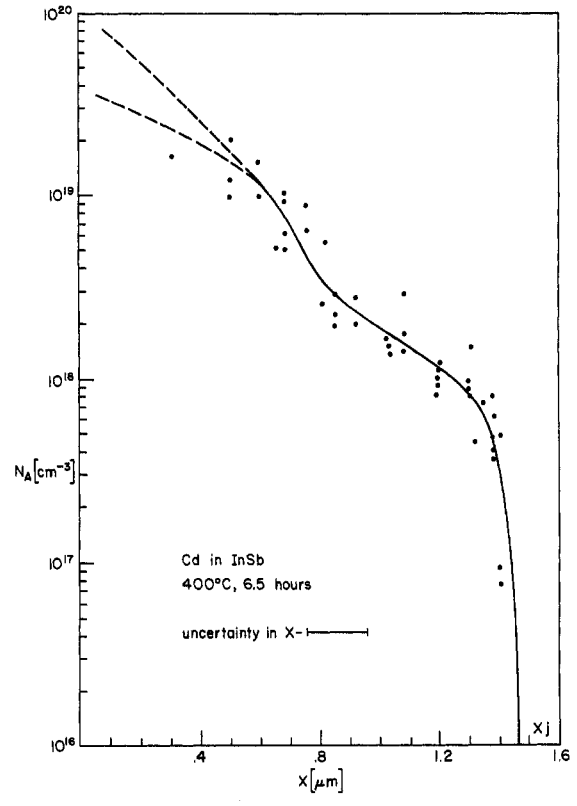

Fig. 2. Diffusion profile of Cd in InSb, measured by the graded $C(V)$ method at 77 K. The uncertainty in the measured value of x is also indicated.

The resulting diffusion profile, showing anomalous behavior commonly found in III-V compounds [1], [7], is given in Fig. 2. The junction depth x_j was inferred from the changing of the $C(V)$ curves' behavior and was confirmed by other methods. The cadmium concentration near the surface was too high to be measured by the $C(V)$ method, so extrapolations to the range of solid solubility are shown. The spread of measured values is mainly due to the waviness of the etched surface Δx_3 of about 0.15 μm in amplitude. Δx_1 was less than 0.07 μm for the lowest measured concentration, and Δx_2 was about 0.05 μm.

Silicon samples were ⟨111⟩-oriented boron-doped wafers of about 10^{15}-cm^{-3} impurity concentration. A layer of 2000-Å thermal oxide was grown on the wafers, and a phosphorus dose of 2×10^{14} cm^{-2} was implanted through it with energy of 250 keV. The thermal oxide served as a mask against out-diffusion in the drive-in step which was carried out for 8 h at 1080°C in nitrogen ambient. After removing the oxide, the samples were gradually etched in a mixture of water, HNO_3,

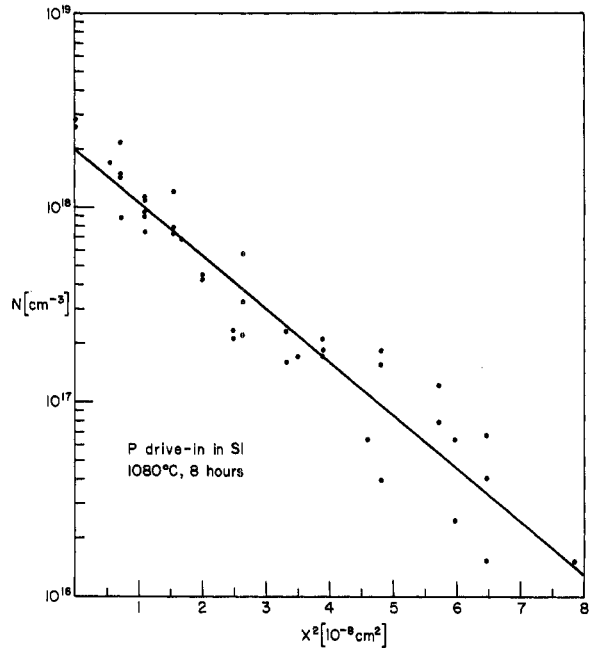

Fig. 3. Concentrations of implanted phosphorus in silicon measured by the graded $C(V)$ method after drive-in diffusion, plotted versus squared depth. The slope of the straight line corresponds to $D = 1.4 \times 10^{-13}$ cm^2/s.

and Hf, leaving a reference step for depth measurements. Subsequent preparation steps were the same as for indium antimonide. We have used pyrolitic SiO_2 and not thermal oxide as an insulator, in order to avoid impurity redistribution during secondary oxidation [4]. The expected phosphorus profile for this single-step diffusion is Gaussian. Measured concentrations are presented in Fig. 3 versus x^2. The slope of a best fitting straight line corresponds to a diffusion coefficient of 1.4×10^{-13} cm^2/s, which is in very good agreement with the literature [2]. The principal source of error is again the nonuniformity of the etching process.

Summary

The use of MOS $C(V)$ method on a gradually etched surface of a diffused semiconductor has been demonstrated as a convenient technique for quick diffusion evaluation. The simple sample preparation process, and easy measurement, and data analysis are the main advantages of this technique. In many cases where handling and processing of semiconductor samples are difficult (InSb at 77 K, for example), the graded $C(V)$ method is much easier than the other electrical techniques. The proposed technique, however, is less accurate than most of the more sophisticated methods and is best utilized for slowly varying profiles and doping levels in the range of 10^{16}–5×10^{18} cm^{-3}.

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Extraction of Average Doping Density and Junction Depth in an Ion-Implanted Deep-Depletion Transistor

DONALD S. WU

Abstract—**A simple model for extracting the average doping density and the junction depth for an ion-implanted deep-depletion device is presented. Reasonable agreement between theory and experiment is shown.**

Introduction

The present available models for measuring the average doping density N_D and the junction depth x_j from the I–V characteristics of an ion-implanted depletion transistor [1], [2] have severe deficiencies for the case of deep-depletion implants with high-energy ions and moderate dosages. They either give substantial errors in both N_D (average doping density), and x_j (junction depth), or are totally inoperable when the surface of the depletion channel fails to achieve an equilibrium inversion layer.

These difficulties are remedied in a new and simple model. The model avoids lengthy mathematical manipulation, and obtains results by looking at the energy-band diagrams of the transistor at different threshold conditions under various substrate biases. The model is limited to a small drain-source voltage.

Theory

Fig. 1 shows the basic structure of an n-channel depletion transistor with proper voltages shown for this discussion. Fig. 2 shows the energy-band diagram of this transistor for the condition that the channel has just been depleted completely.

The symbols are defined below:

ϕ_B > 0 p-n junction built-in potential.

$$x_n = \sqrt{\frac{2\epsilon_{Si}}{qN_D}\left(\frac{N_A}{N_D + N_A}\right)(\phi_B - V_{BS})}$$ n-side depletion width due to V_{BS}.

$$x_d = \frac{\epsilon_{Si}}{C_{ox}}\left(\sqrt{1 - \frac{2(V_{Tn} - V_{FB})}{V_0}} - 1\right)$$ surface depletion width due to V_{GS}.

V_{FB} Flat-band voltage referenced to source.

$$V_0 = \frac{\epsilon_{Si} q N_D}{C_{ox}^2}.$$

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