a short-term test turning on from 1750 V. (During normal operation, the turn-on voltage would not exceed 1100 or 1200 V and would usually be about 300 V.) This test was of 1-min duration with the junction temperature at 105°C.

Table III shows a more complete picture of the latest *di/dt* tests and show, for example, that device type 4 is more robust than the type 3 devices. Letters *A*, *B*, *C*, and *D* denote subtype device variations which, like the design theory and design details, will be dealt with in a later paper. From this table it would be tempting to rate the device at these *di/dt* values. However, the test is a stress test and 160 A/μs at 1750 V for 1 min must be reduced to smaller ratings for continuous operation. For example, with a device of this type one might expect 80 h of safe operation turning on from 1200 V at 100 A/μs or 12 years turning on from 800 V at a *di/dt* of 75 A/μs.

VI. Conclusion

A series of light-fired devices has evolved with EPRI support. These range from the EPRI-GE1 to the EPRI-GE4. All of these devices retained the 2000-V/μs *dV/dt*, the low forward drop, the blocking voltage (2600 V), and the current rating (1000 A) of the original electrically fired device. These devices have all had at least two amplifying stages to achieve safe turn-on from a typical incident gate photo energy of 30 nJ. Experimental results and turn-on models capable of incorporating amplifying stage characteristics have led to improved designs from the GE1 with its poor high-temperature turn-on capability to the GE4 which rivals its electrical counterpart despite a 6 to 1 initial turn-on line disadvantage and a 100 to 1 smaller input gate energy. These results indicate that a one-for-one replacement of electrically fired devices and their costly and high parts content firing systems with a direct light-fired device is at least technically feasible at voltages up to 2600 V. Further work is being carried out to investigate total system cost factors and possible suitability at higher voltages.

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n-Channel MOS Transistors in Mercury–Cadmium–Telluride

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Abstract—**n-channel MOS transistors operating at 77 K have been realized in $Hg_{0.71}Cd_{0.29}Te$ with ion-implanted source and drain junctions. Enhancement-mode transistors were made with evaporated ZnS as a gate insulator, and depletion-mode transistors were made using a native oxide of mercury-cadmium-telluride. The devices exhibit surface mobility as high as 1.5×10^4 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Current-voltage characteristics and capacitance-voltage data are presented and analyzed.**

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Introduction

THE MONOLITHIC APPROACH [1] to infrared imaging has motivated research on active electron devices in narrow-bandgap semiconductors. Significant progress has been made in recent years in the technology of the adjustable-bandgap semiconductor $Hg_{1-x}Cd_xTe$ [2]. Photovoltaic quantum detectors [3], [4] and charge-coupled devices (CCD's) [5] have been made in addition to the more common photoconductors. The MOS transistor is a device suitable for inte-

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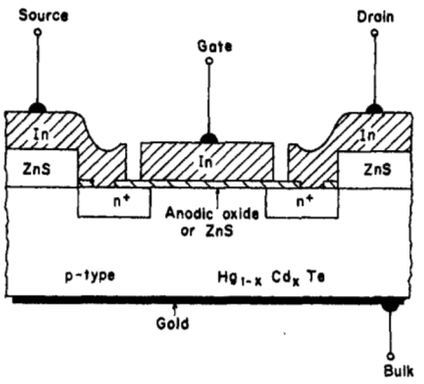

Fig. 1. Mercury-cadmium-telluride MOS transistor structure.

gration with photodiodes, and it has potential uses for signal switching and CCD interfacing [6].

This work describes experimental n-channel $Hg_{1-x}Cd_xTe$ MOS transistors with ion-implanted junctions. $Hg_{1-x}Cd_xTe$ is a compound semiconductor [7]. For the composition $x = 0.29$ the bandgap at 77 K is 0.235 eV. This material is useful for detection of infrared radiation in the 3-5-μm spectral range. The band structure is asymmetric and leads to a very high electron-to-hole mobility ratio, of the order of 150. The bulk electron mobility is typically 3×10^4 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1} at 77 K. Two types of transistors have been realized, utilizing different materials for the gate insulator: depletion-mode devices were made with native oxide of $Hg_{1-x}Cd_xTe$, characterized by a positive interface charge density Q_{ss}/q of the order of 10^{12} cm^{-2}; enhancement-mode devices were made with ZnS insulation, characterized by interface charge density about 10^{11} cm^{-2}, which is less than the depletion-layer charge necessary for surface inversion. The following sections describe the $Hg_{1-x}Cd_xTe$ transistor structure and discuss interface properties.

Device Structure

The transistors are made of single-crystal p-type $Hg_{0.71} \cdot Cd_{0.29}Te$ with hole concentration of about 5×10^{15} cm^{-3}, determined by native defects. Fig. 1 illustrates the device structure. Source and drain n-type regions are formed by ion implantation of boron. Conversion to n-type is caused by implantation damage, thus the identity and dose of the implanted species are not very significant [8]. The gate insulator is either anodic oxide of $Hg_{1-x}Cd_xTe$ or a thin layer of ZnS. Field insulation and surface passivation outside the active gate region are provided by thick ZnS. Indium metallization serves for contacting the implanted areas and forms the metal gate. A rear-side gold contact is used as the bulk terminal.

Depletion-Mode MOS Transistors

Current-voltage characteristics of a transistor with native oxide gate insulator are shown in Fig. 2. The device displays classical MOS characteristics with clear ohmic and saturation regions. For each gate voltage V_{GS}, the current begins to saturate at a drain voltage $V_{D_{sat}} = V_{GS} - V_T$, where the threshold voltage V_T is about -1.5 V. In Fig. 2(c), the ohmic-region current I_{DS} is plotted versus gate voltage for $V_{DS} = 40$ mV and $V_{BS} = 0$. The data fit the well-known approximate relation [9]

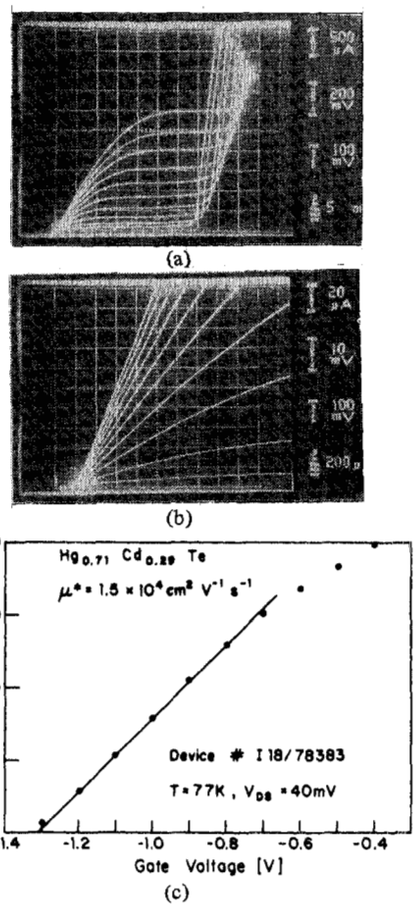

Fig. 2. I-V characteristics of n-channel $Hg_{0.71}Cd_{0.29}Te$ MOS transistor with native oxide gate insulator at 77 K, measured with $V_{BS} = 0$. Device parameters: $Z = 200$ μm, $L = 60$ μm, $C_{ox} = 1.3 \times 10^{-7}$ F $\cdot$ cm^{-2}, $N_A = 3.3 \times 10^{15}$ cm^{-3}, $t_{ox} = 1400$ Å, $\epsilon_{ox} = 20$. (a) Full characteristics with gate voltages -1.2, -1.1, $\cdots$, -0.3 V. (b) Characteristics in the ohmic region for gate voltages -1.3, -1.2, $\cdots$, -0.4 V. (c) Drain current versus gate voltage in the ohmic region for $V_{DS} = 40$ mV.

$$I_{DS} = C_{ox}\mu^* \frac{Z}{L} (V_{GS} - V_T) V_{DS} \tag{1}$$

with a threshold-voltage intercept of -1.31 V. This value corresponds to a flat-band voltage $V_{FB} \simeq V_T - 2\phi_F - Q_B/C_{ox}$ of -1.75 V, indicating the presence of a positive interface charge of approximately

$$\frac{Q_{ss}}{q} \simeq \frac{1}{q} C_{ox} V_{FB} = 1.4 \times 10^{12} \text{ cm}^{-2}. \tag{2}$$

This is in agreement with values observed by other methods [10], [11]. In the above we have neglected the effect of ϕ_{MS}, the metal-semiconductor work function difference, since the effect of the large interface charge is predominant [10]. From the slope $\Delta I_{DS}/\Delta V_{GS}$ at low currents an electron mobility μ^* at the surface of 1.5×10^4 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1} is calculated. This value is 30-50 percent of the electron mobility in bulk material of the same composition [7]. The device is characterized by a very high gain parameter $\beta_0 = C_{ox}\mu^* = 2 \times 10^{-3}$ A $\cdot$ V^{-2}, due to the high dielectric constant of the oxide

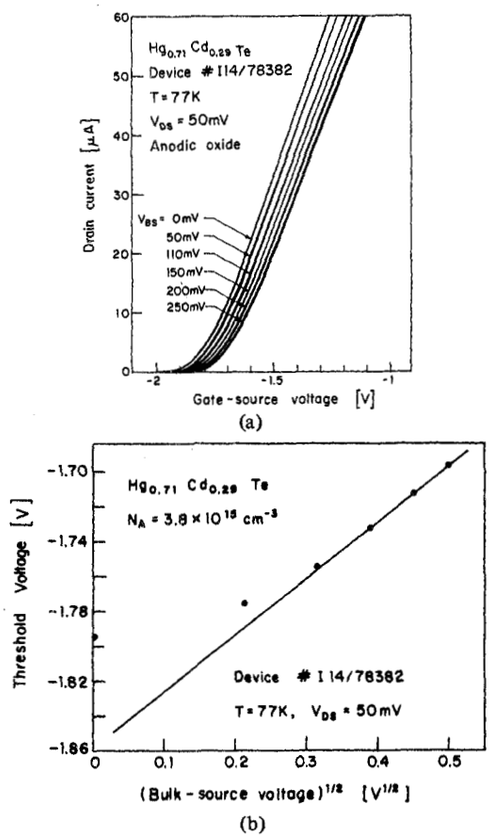

Fig. 3. Drain current versus gate voltage for depletion-mode transistor with $Z = 172\ \mu m$, $L = 80\ \mu m$, $C_{ox} = 1.73 \times 10^{-7}$ F · cm^{-2}, $t_{ox} = 1000$ Å, $\epsilon_{ox} \simeq 20$, $N_A = 3.8 \times 10^{15}$ cm^{-3}, at 77 K. (a) Ohmic region characteristics for bulk-source biases $V_{BS} = 0, -10, -50, -110, -150, -200$, and -250 mV. (b) Threshold voltages obtained from the intercepts of (a) plotted versus V_{BS}, exhibiting the effect of the depletion charge Q_B.

($\epsilon_{ox} = 20$) [12] and the high effective mobility. In the saturation region, the current is proportional to $(V_{GS} - V_T)^2$, as expected from simplified theory [9].

A more exact analysis is given in Fig. 3 for a similar device. Drain current I_{DS} in the ohmic region was recorded versus gate voltage V_{GS} for several values of bulk-source reverse bias V_{BS}. By extrapolation of the curves to zero current, the threshold voltage is obtained for each value of V_{BS}. The data fit the relation [9]

$$V_T = V_{T_0} + \frac{\sqrt{2\epsilon\epsilon_0 qN_A}}{C_{ox}}\sqrt{2\phi_F + |V_{BS}|} \simeq V_{T_0} + K\sqrt{|V_{BS}|} \tag{3}$$

with $V_{T_0} = -1.854$ V and $K = 0.322$. The theoretical value of the constant K, calculated using the device parameters, is 0.245. This dependence represents the effect of the depletion charge Q_B, induced by V_{BS}, on the threshold. The effective mobility is calculated from the slope of these curves, and is of the order of 8.2×10^3 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1}. It is seen that the increased normal surface field due to V_{BS} causes a decrease in surface mobility.

Electrical breakdown of the drain-bulk junction occurs at a reverse bias of about 1.4 V, and is affected by the gate voltage,

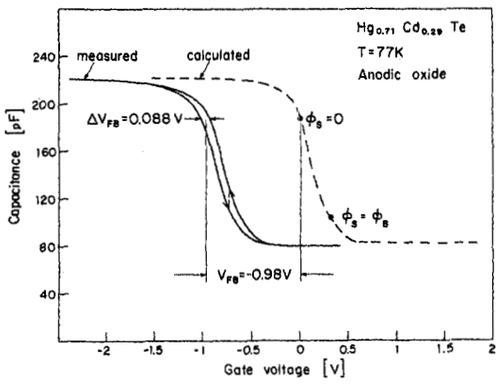

Fig. 4. C-V characteristics of MOS capacitor with 820-Å anodic oxide on p-type $Hg_{0.71}Cd_{0.29}Te$. $N_A = 3.5 \times 10^{16}$ cm^{-3}, $A = 1.024 \times 10^{-3}$ cm^2, $T = 77$ K, $f = 1$ MHz.

as shown in Fig. 2(a). The breakdown voltage behaves approximately as $BV = BV_0 + mV_G$, with $m = 2/3$ [9]. In some devices, photocurrent multiplication was observed when the junction was operated as a reversed-biased photodiode. Devices made on substrates with higher impurity concentrations ($N_A > 10^{16}$ cm^{-3}) exhibit soft breakdown at lower bias, especially at gate voltages which cause both accumulation on the p-type surface and inversion of the surface of the n-type implanted regions. Such transistors are limited in operating voltages by tunneling of electrons from the valence band of the inversion layer to the conduction band of the n-type implanted layer [8].

The interface charge Q_{SS} and the surface state density n_{SS} under the gate region were determined using MIS capacitors by established C-V techniques. High-frequency C-V data for the indium-native oxide-$Hg_{0.71}Cd_{0.29}Te$ MIS structure are presented in Fig. 4. The flat-band voltage is -0.98 V, corresponding to a fixed interface charge density of approximately 1.3×10^{12} cm^{-2}, in good agreement with measured transistor threshold voltage. The measured hysteresis is caused by trapping of minority carriers at the interface. The hysteresis shift in flat-band voltage ΔV_{FB} corresponds to a trap density of

$$N_{st} \simeq \frac{C_{ox}\Delta V_{FB}}{q} = \frac{2.17 \times 10^{-7} \times 0.088}{1.6 \times 10^{-19}} = 1.6 \times 10^{11}\ \text{cm}^{-2}. \tag{4}$$

When the gate bias swing is reduced, the hysteresis loop shrinks, indicating a reduction in trapping. The number of fast surface states is found from the slope of the C-V curve in comparison with the ideal curve, by the differentiation method [13], i.e.,

$$n_{SS} = -\frac{1}{q}\left(\frac{\partial Q_{SS}}{\partial \phi_s}\right) = -\frac{C_{ox}}{q}\frac{\partial}{\partial \phi_s}(V_{G\,\text{meas}} - V_{G_i}) = \frac{C_{ox}}{q}\left[\frac{1}{\dfrac{\partial C}{\partial V_G}\Big|_i} - \frac{1}{\dfrac{\partial C}{\partial V}\Big|_{\text{meas}}}\right]\cdot\frac{\partial C}{\partial \phi_s}. \tag{5}$$

The midgap surface state density must be calculated from the slopes at $\phi_s = \phi_F$. In this neighborhood, the measured curve is fairly parallel to the ideal curve, so that the differentiation

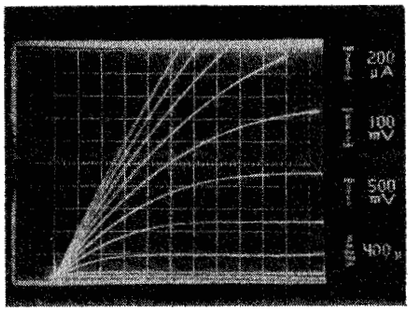

Fig. 5. I-V characteristics of n-channel $Hg_{0.71}Cd_{0.29}Te$ MOS transistor with ZnS gate insulator, measured at 77 K with $V_{BS} = 0$. Device parameters: $Z = 200\ \mu m$, $L = 60\ \mu m$, $N_A = 3.3 \times 10^{15}\ cm^{-3}$, $C_{ZnS} = 2.3 \times 10^{-8}\ F \cdot cm^{-2}$, $t_{ZnS} = 2890$ Å, $\epsilon_{ZnS} = 7.5$. Gate voltages are 0, 0.5, 1, 1.5, $\cdots$, 4.5 V.

method is not sufficiently accurate, but it may be safely concluded that the fast state density is less than $5 \times 10^{11}\ cm^{-2} \cdot eV^{-1}$ at midgap. Moving from midgap towards the valence band (i.e., towards flat band and accumulation) the deviation in slope between the measured and the ideal curve increases continuously, yielding surface-state densities in the range 10^{12} to $10^{13}\ cm^{-2} \cdot eV^{-1}$. The total number of fast states in the lower half of the bandgap is at least $\Delta V_{ss} C_{ox}/q \simeq 1.5 \times 10^{11}\ cm^{-2}$, where ΔV_{ss} is the extra gate voltage required to reach accumulation from midgap. Information about the upper side of the bandgap ($\phi_s > \phi_F$) cannot be obtained from this curve; analysis of high-frequency C-V plots on n-type samples leads to the same conclusions concerning the upper half of the energy gap. Similar results, calculated from low-frequency C-V methods, have previously been reported for this interface [10], [11].

Enhancement-Mode MOS Transistors

The characteristics of a transistor with ZnS gate insulator are shown in Figs. 5 and 6. The measured gate capacitance is $2.3 \times 10^{-8}\ F \cdot cm^{-2}$. Using a value of 7.5 for the dielectric constant of ZnS at liquid nitrogen temperature [14], the thickness of the evaporated ZnS film is calculated to be 2890 Å. The lower gate capacitance causes the transistor to have a lower transconductance in comparison with the anodic oxide device and saturation is reached at drain voltages lower than $V_{GS} - V_T$, due to the depletion-layer charge Q_B (body effect). We have verified that these characteristics fit the classical MOS model [15]

$$I_{DS} = C_{ox}\mu^* \frac{Z}{L} \left\{ [V_{GS} - V_{FB} - 2\phi_F - 0.5\ V_{DS}]\ V_{DS} - \frac{2}{3} \frac{\sqrt{2\epsilon_0 \epsilon_s q N_A}}{C_{ox}} \cdot [(V_{DS} + V_{SB} + 2\phi_F)^{3/2} - (V_{SB} + 2\phi_F)^{3/2}] \right\}. \quad (6)$$

At high gate voltages μ^* should be modified in (6) to account for the reduction in surface mobility due to vertical field, which is clearly observed in Fig. 6. The threshold voltage is 50 mV, indicating a low-interface charge density of the order of $10^{11}\ cm^{-2}$. In contrast with the anodic oxide interface

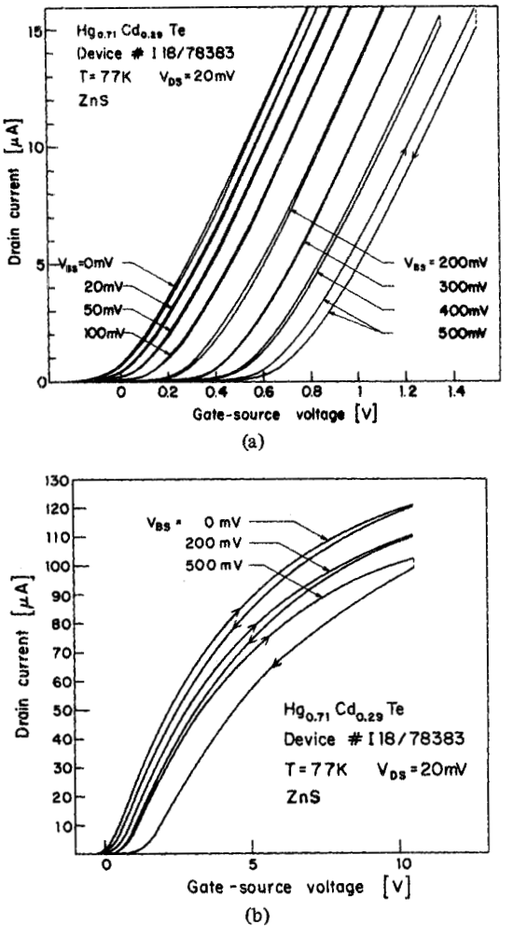

Fig. 6. Drain current versus gate voltage for the device of Fig. 5, measured at 77 K with $V_{DS} = 20$ mV, for various values of bulk-source bias V_{BS}. (a) Low-current region. $\mu^* = 14\ 000\ cm^2 \cdot V^{-1} \cdot s^{-1}$. (b) High-current region, showing pronounced hysteresis and decrease of mobility with electric field.

charge, which causes strong inversion, this charge is not sufficient to cause inversion, and hence the surface is depleted to some extent ($Q_{ss}/q = +10^{11}\ cm^{-2} < Q_B/q = 2 \times 10^{11}\ cm^{-2}$ for $\phi_s = 2\phi_F$, $N_B = 10^{16}\ cm^{-3}$).

The characteristics of Fig. 6 exhibit hysteresis. This is caused by electron trapping at the interface. The hysteresis is pronounced at high gate voltages and at reverse source-bulk bias V_{BS}. The effect is accompanied by a reduction of surface mobility, as can be seen from the slopes of Fig. 6. Also evident in Fig. 6 is the increase in threshold voltage caused by reverse bulk-source voltages.

The transistor parameters described above are consistent with C-V data for an MOS capacitor with about 2250-Å ZnS insulation, shown in Fig. 7. The C-V curve exhibits a hysteresis width of about 0.5 V, corresponding to a trap density of about $10^{11}\ cm^{-2}$. This is not the total number of traps, since the width of the hysteresis loop may be increased by applying a larger-amplitude bias sweep. The surface is seen to be depleted at zero voltage. It is impossible to locate the flat-band voltage, since it depends on trap occupancy. The difference in slopes between the measured and the ideal curves gives

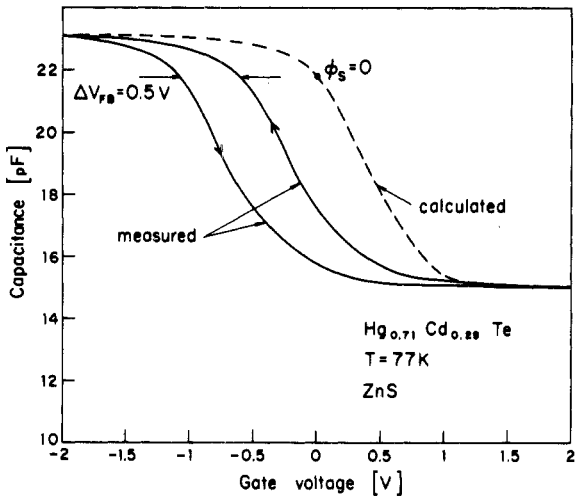

Fig. 7. *C-V* characteristics of MOS capacitor with 2250-Å ZnS on p-type $Hg_{0.71}Cd_{0.29}Te$. $N_A = 5.6 \times 10^{15}$ cm^{-3}, $A = 7.84 \times 10^{-4}$ cm^2, $T = 77$ K, $f = 1$ MHz.

fast state densities in the order of 10^{11} cm$^{-2} \cdot$ eV^{-1} near midgap, and a total of at least 10^{11} cm^{-2} states throughout the energy gap.

Conclusion

In summary, we have shown the feasibility of high-transconductance MOS transistors in $Hg_{1-x}Cd_xTe$. Both ZnS and anodic oxide have good interfaces with $Hg_{1-x}Cd_xTe$. The higher dielectric constant of the anodic oxide allows the inversion charge to be induced at lower electric field, so that the effects of surface states and traps are diminished. The main drawback of the native oxide device is the fixed positive interface charge which forms a conducting channel at zero gate voltage, thus creating circuit complications if on/off switching is required. Many aspects of the devices, such as noise, remain yet to be studied.

Acknowledgment

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